

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/748,551

Confirmation No.

First Inventor: Joseph B. Rowlands

Filed: 12/30/2003

Art Unit: 2186

Examiner:

Title: Direct Access Mode For A Cache

Continuation of 09/633,544; filed 08/07/2000; now US Patent 6,732,234

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicant submits the attached Information Disclosure Statement and requests the Examiner to consider the listed references. All of the references noted on this IDS were submitted on Form PTO-1449 by the Applicant or cited by the Examiner in the parent case, noted above. Thus, copies of the references are in the parent case.

It is certified, to the best of knowledge, this IDS is being submitted before the mailing date of a first Office Action on the merits. However, if there are any fee shortages related to this submission, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

GARLICK, HARRISON & MARKISON, LLP
(Customer No. 34,399)

Date: 7-23-04

By: William W. Kidd

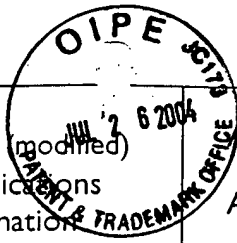
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**Form PTO-1449** (modified)

List of Patents and Publications
For Applicant's Information
Disclosure Statement
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ATTY. DOCKET NO: *BP1735CON*SERIAL NO: *10/748,551*APPLICANT: *JOSEPH B. ROWLANDS*GROUP: *2186*FILING DATE: *12/30/2003***U.S. PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	3,693,165	9/1972	Reiley et al.			
	A2	5,416,783	5/1995	Broseghini et al.			
	A3	5,450,551	9/1995	Amini et al.			
	A4	4,511,994	4/1985	Webb et al.			
	A5	4,633,440	12/1986	Pakulski			
	A6	4,654,778	3/1987	Chiesa et al.			
	A7	4,907,278	3/1990	Cecinati et al.			
	A8	5,241,663	8/1993	Rohwer			
	A9	5,325,504	6/1994	Tipley et al.			
	A10	5,317,716	5/1994	Liu			
	A11	5,510,934	4/1996	Brennan et al.			
	A12	5,551,001	8/1996	Cohen et al.			
	A13	5,592,679	1/1997	Yung			
	A14	5,644,752	7/1997	Cohen et al.			
	A15	5,668,815	9/1997	Gittinger et al.			
	A16	5,668,972	9/1997	Liu et al.			
	A17	5,748,640	5/1998	Jiang et al.			
	A18	5,768,555	6/1998	Tran et al.			
	A19	5,784,588	7/1998	Leung			
	A20	5,802,338	9/1998	Rechtschaffen et al.			
	A21	5,809,528	9/1998	Miller et al.			
	A22	6,161,167	12/2000	Witt			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

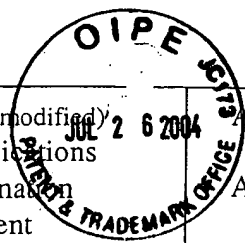
	A23	Dekker et al., "A Realistic Fault Model and Test Algorithms for Static Random Access Memories," IEEE Transactions on Computer-Aided Design, Vol. 9, No. 6, June 1990, pp. 567-572.
	A24	Halfhill, "SiByte Reveals 64-bit Core for NPUs," Microprocessor Report, June 2000, pp. 45-48.
	A25	Cyrix® 5x86 Microprocessor, July 1995, 8 pgs.
	A26	Cyrix® 6x86 Microprocessor, August 1995, 6 pgs.

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DATE CONSIDERED:

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GROUP: **2186**

U.S. PATENT DOCUMENTS

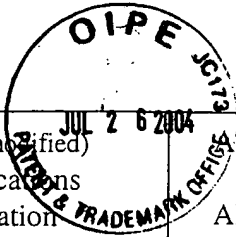
EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	B1	4,044,338	8/1977	Wolf			
	B2	4,453,212	6/1984	Gaither et al.			
	B3	4,807,115	2/1989	Tornig			
	B4	4,858,105	8/1989	Kuriyama et al.			
	B5	5,125,083	6/1992	Fite et al.			
	B6	5,163,142	11/1992	Mageau			
	B7	5,226,126	7/1993	McFarland et al.			
	B8	5,226,130	7/1993	Favor et al.			
	B9	5,353,425	10/1994	Malamy et al.			
	B10	5,377,345	12/1994	Chang et al.			
	B11	5,432,918	7/1995	Stamm			
	B12	5,471,598	11/1995	Quattromani et al.			
	B13	5,487,162	1/1996	Tanaka et al.			
	B14	5,526,510	6/1996	Akkary et al.			
	B15	5,557,763	9/1996	Senter et al.			
	B16	5,588,126	12/1996	Abramson et al.			
	B17	5,638,537	6/1997	Yamada et al.			
	B18	5,761,712	6/1998	Tran et al.			
	B19	5,913,224	6/1999	MacDonald			
	B20	6,240,432	5/29/01	Chuang, et al.			
	B21	6,263,082	7/17/01	Ishimoto, et al.			
	B22	6,237,083	5/22/01	Favor			
	B23	5,564,034	10/8/96	Miyake			
	B24	5,875,465	2/23/99	Kilpatrick, et al.			
	B25	4,833,642	5/23/89	Ooi			
	B26	6,351,789	2/26/02	Green			
	B27	5,584,014	12/10/96	Nayfeh, et al.			
	B28	5,974,507	10/26/99	Arimilli, et al.			

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GROUP: 2186

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FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	B29	0 061 570	10/1982	EP			
	B30	0 259 095	3/1988	EP			
	B31	0 381 471	8/1990	EP			
	B32	0 436 092	7/1991	EP			
	B33	0 459 232	12/1991	EP			
	B34	0 459 233	12/1991	EP			
	B35	0 568 221	11/1993	EP			
	B36	0 687 979	12/1995	EP			
	B37	2 263 985	8/1993	GB			
	B38	2 263 987	8/1993	GB			
	B39	2 281 422	3/1995	GB			

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B40	Intel® StrongARM® SA-1100 Microprocessor, Developer's Manual, August 1999, © Intel Corporation, Ch. 1, p. 6; Ch. 2, p. 2; Ch. 6, pp. 2-5; Ch. 7, p. 3.
B41	"Memory Arbitration with Out of Order Execution in Conjunction with a RISC System," IBM Technical Disclosure Bulletin, September 1992, pp. 62-64.
B42	"Handling Reservations in Multiple-Level Cache," IBM Technical Disclosure Bulletin, December 1993, pp. 441-446.
B43	Stepanian, SiByte, "SiByte SB-1 MIPS64 CPU Core, Embedded Processor Forum 2000, June 13, 2000, 15 pages.

EXAMINER:

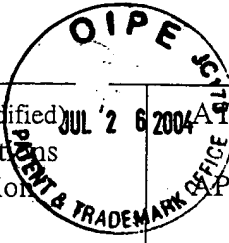
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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	D1	5,493,667	2/20/96	Huck, et al.			
	D2	5,586,293	12/17/96	Baron, et al.			
	D3	5,809,531	9/15/98	Brabandt			
	D10	5,983,321	11/9/99	Tran, et al.			
	D11	5,671,444	9/23/97	Akkary, et al.			
	D12	6,269,427	7/31/01	Kuttanna, et al.			
	D13	6,295,608	9/25/01	Parkes, et al.			

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	D4	325 420	7/26/89	EP			
	D5	997 821	5/3/00	EP			
	D6	2 214 336	8/31/89	GB			

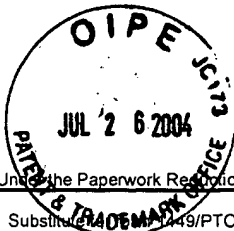
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	D7	Gallup, et al., "Testability Features of the 68040," Motorola, Inc., 1990 International Test Conference, IEEE, pp. 749-757.
	D8	Hollenbeck, et al., "PA7300LC Integrates Cache for Cost/Performance," Hewlett Packard Company, IEEE, 1996, pp. 167-174.
	D9	International Search Report for EP 26 231-50 mailed February 21, 2003, 7 pages.

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PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

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STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/748,551
Filing Date	12/30/2003
First Named Inventor	Joseph B. Rowlands
Art Unit	2186
Examiner Name	
Attorney Docket Number	BP1735CON

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	E1	US- 5,752,261	05-1998	Cochcroft, Jr.	
	E2	US- 5,787,490	07-1998	Ozawa	
	E3	US- 5,193,163	03-1993	Sanders et al.	
	E4	US- 6,115,792	09-2000	Tran	
	E5	US- 6,240,532	05-2001	Cho	
	E6	US- 6,148,370	11-2000	Kobayashi	
	E7	US- 5,539,878	07-1996	Kikinis	
	E8	US- 4,996,641	02-1991	Talgam et al.	
	E9	US- 4,575,792	03-1986	Keeley	
	E10	US- 5,586,253	12-1996	Green et al.	
	E11	US- 6,185,703	02-2001	Guddat et al.	
	E12	US- 5,524,208	06-1996	Finch et al.	
	E13	US- 6,606,686	08-2003	Agarwala et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ *Number ⁴ *Kind Code ⁵ (if known)				

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